Contamination sources and elimination

The ongoing trend to push high-efficiency PV cell devices to higher efficiency levels is more and more accompanied by the adaption of semiconductor device fabrication standards. One of the reasons is the rising sensitivity of p-i-n PV cell structures of thin film layer stacks to the impact of impurities, which may be increasingly harmful with respect to the proper functionality of the layers themselves or their surface interaction.

Therefore, suitable measures have to be implemented to suppress such film contamination in the manufacturing process. From the equipment point of view, it is highly desirable to avoid potential contamination sources upfront and to implement efficient treatments for avoiding so-called memory effects.

One such successful design is Indeotec's PECVD Mirror Reactor, specifically for manufacturing HJT devices. It eliminates the need for wafer flipping and so removing the potential flipping automation contamination source.

Additionally, Indeotec successfully tested a plasma treatment method which means it's possible to process the intrinsic and the subsequent doped a-Si:H layer in one reactor, which could reduce the number of required deposition chambers by half.

Sources of contamination

Since the cleanliness of the device fabrication process will receive an ever-increasing attention it is useful to identify the impurity sources and their present and future significance. The research work done by the semiconductor industry will serve as a guideline in structuring the contamination sources[1]. The following table shows the survey.

1 Baltzinger, Jean-Luc, Delahaye, Bruno: Contamination monitoring and analysis in semiconductor manufacturing. Altis Semiconductor, France. Article published in book "Semiconductor Technologies", InTech 2010.

Foreign or unwanted materials		Parasitic reactions	
1	Impurities contained in fluid: Gases, chemicals	4	Impurity products originated by reactive materials
2	Impurities originated by tools: Corrosion, outgassing, handling	5	Corrosion, dissolution of tools parts
3	Particles: Suspension within fluids, abrasion		

Table 1

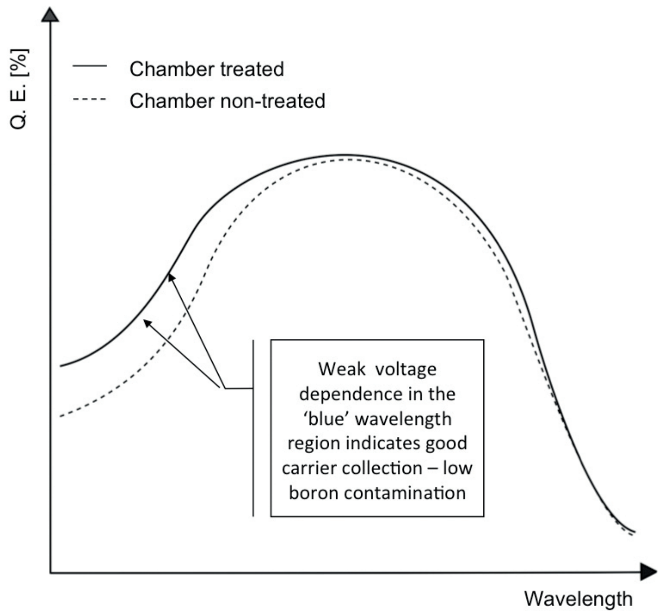

Figure 1: Principal graph of impact of dopant contamination at the quantum efficiency of a HJT cell device

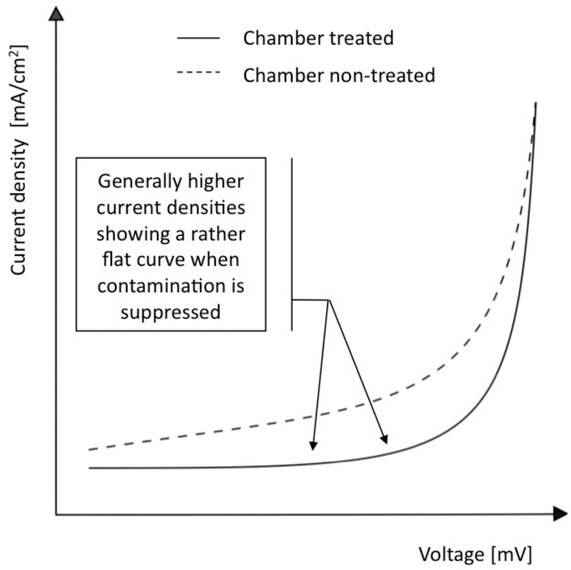

Figure 2: Principal graph of impact of dopant contamination at the I-V characteristics of a HJT cell device

In terms of transport of the contaminants these phenomena have to be considered:

Brownian movement

Convection

Molecular diffusion

Electromagnetic diffusion

For the PECVD deposition of the intrinsic and doped a-Si:H thin films, it was observed that predominantly surface contamination effects by dopants showed a remarkable impact on the device film quality. Such dopants remained (1) in the equipment at the reactor chamber walls, or (2) were carried on with the supporting tray. In table 1 above this is shown in 2 and 5. In the future and with efficiency levels rising, item 1, process gas purities, may be considered more.

Particle contamination, item 3, will have an impact if the deposited tool parts have not been cleaned properly or the cleaning cycles were too long. Such cleaning processes, for example dry etching with NF3, may be carefully monitored in the production and may become more critical with rising efficiencies.

Impact of cross-contamination at the device properties

For an HJT structure with an i-p layer at the top and an i-n layer stack at the bottom the critical contamination takes place when the intrinsic layer is deposited at the silicon bulk layer, but the dopants, which remained at the chamber walls from the previous deposition cycle or even in the tray, will be incorporated in this layer also. Such incorporation leads to a considerable drop in the QE curve and will be also clearly visible in the I-V plots, see figures 1 and 2.

A contaminated interface between the bulk Si and the intrinsic a-Si:H layer results in an insufficient carrier separation and thus a less efficient collection in the PV cell device. The special effect of boron contamination is known from the single-chamber device deposition of amorph/micromorph silicon thin film p-i-n layer stacks. However, the effects are different on HJT cell architectures and the treatments of boron contamination cannot be adopted straight away.

Treatment approach and results

Indeotec tested various dopant removal treatment approaches of dry cleaning, including a plasma chamber treatment procedure, which is inexpensive and short

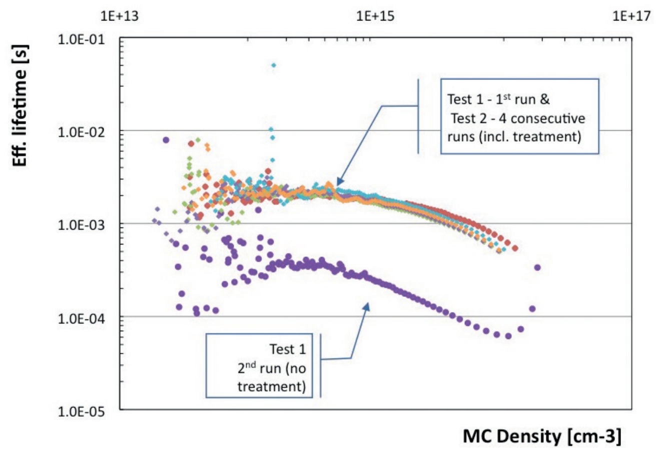

Figure 3: Graph of minority carrier lifetime. Test 1 shows the 2nd run after non-treatment of the chamber. Test 2 shows 4 deposition cycles, with chamber treatment in between the cycles

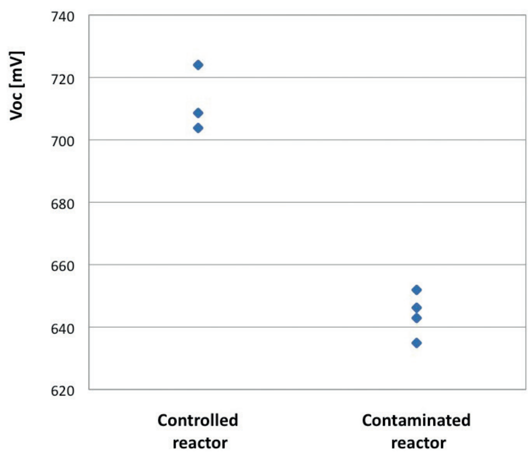

Figure 4: Graph of VOC illustrating the difference between the treated and non-treated reactor chamber treatment in between. Kindly note that the passivation recipe was not optimized for these tests.

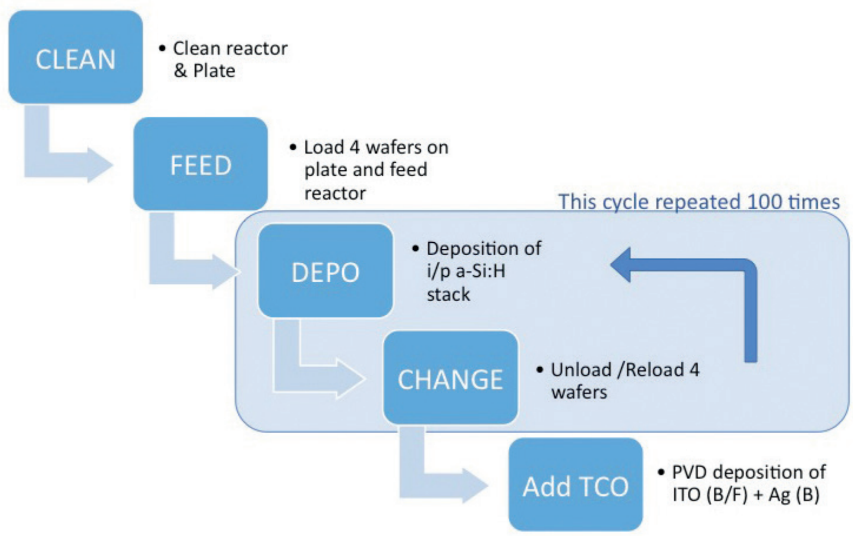

Figure 5: Chart of the process steps for the multi-cycle, long-term treatment test for both the deposition chamber and the wafer carrier

enough, in terms of an acceptable treatment time between the deposition runs.

An initial test comprising a couple of deposition cycles had the objective to identify immediate effects of a potential cross contamination originated by the reactor walls. For this purpose, the critical i-p deposition sequence was selected. Test 1 was conducted as follows: between 2 cycles the PECVD chamber was not treated. Test 2 had this procedure: for running 4 cycles in a sequence, the chamber was treated in between the depo cycles.

All tests were executed in an OCTOPUS II PECVD system using one PECVD chamber. The results show an immediate and significant reduction of the key parameters already in the 2nd deposition cycle; when the reactor wasn't treated before, see figures 3 and 4. Immediately, in the repetition cycle, the minority carrier lifetime is almost one order of magnitude lower (figure 3). The VOC is reduced by 10 -15% (figure 4). In contrast, when the chamber treatment is applied, the curves of the lifetime overlap almost completely, which indicates an efficient removal of the impurities. This was monitored for 4 cycles in a row, Figure 4.

A second tests series should confirm the effectiveness of the dopant removal treatment for both sources, reactor walls and the supporting tray. The deposition of an i-p-deposition stack was monitored and repeated 100 times in order to detect potential impurity accumulation effects, which may occur in the long run. It is assumed that after 100 runs there will be a wall cleaning of the reactor by etch removal. In an optimised production environment, this may be further prolonged in order to tweak the overall uptime.

For obtaining real I-V curve parameters and ultimately, efficiency data, all cell devices were completely processed: top and bottom PECVD layers, top and bottom TCO deposition, contacting. Plus, for the last deposition cycle of the series (test run #100) the wafer supporting tray, which had been coated as many times as the reactor walls, was replaced by a new one, in order to identify a potential difference. Between the cycles 1-99 the tray was also treated. The complete test sequence is illustrated in figure 5.

For the PECVD process step – passivating and device generation – the Minority carrier lifetime was measured and evaluated, the implied values of VOC (iVOC) and fill factor (iFF) derived. The compound summary of minority carrier lifetime results are illustrated in figure 6.

Across all 100 runs the values of the lifetime remained at a consistently stable level. A slight improvement could be observed when a clean tray was used for run #100. No immediate or gradual degradation of the passivation characteristics could be seen, no accumulation of contaminants was monitored.

Obviously, the applied treatment method removes any potential dopant contaminants from both the reactor walls and the tray in a highly efficient way. The further processing of the precursors to complete PV cell devices, was conducted with the objective of obtaining real, comparable I-V and efficiency data and to confirm the trend which was detected during the passivation step. Figure 7 illustrates the results for the VOC as a representative value. The measured data confirms consistently stable and high parameter levels. Again, this set of parameter measurements confirms the effectiveness of the dopant removal methods.

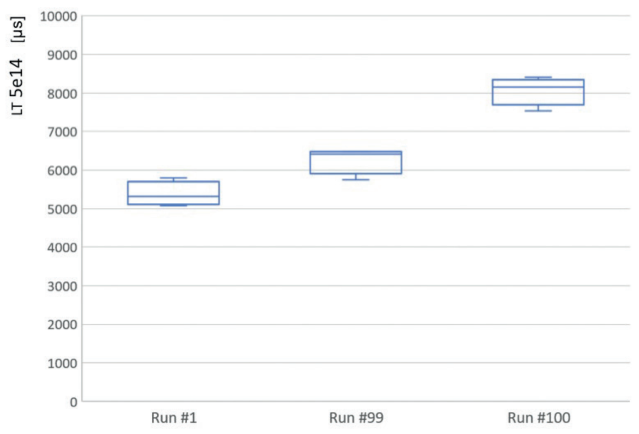

Figure 6: Box plot of minority carrier lifetime trend for the marathon test. The treatment procedure maintains the LT levels throughout all runs.

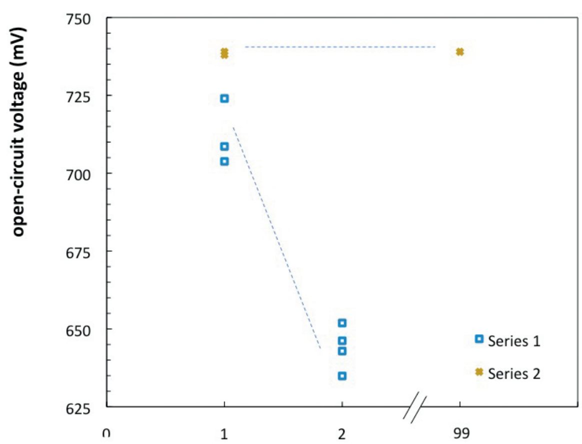

Figure 7: Plot of VOC data points for the 100-test (series 2). The data points for the VOC from the initial test (series 1) illustrate the immediate and drastic effect of non-treatment.

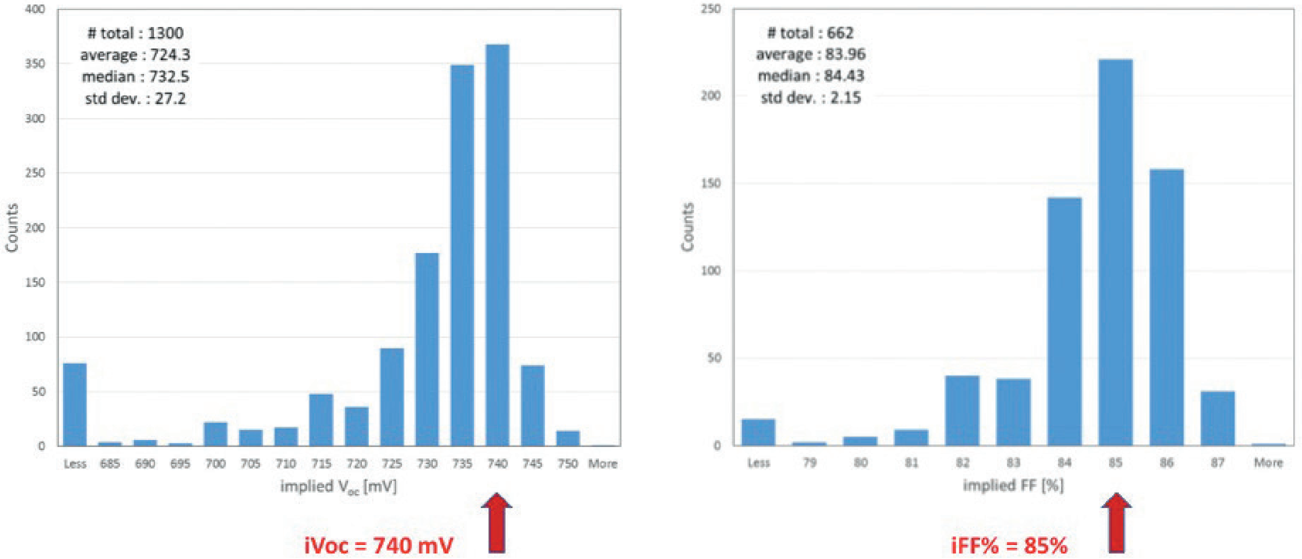

Figure 8: Chart of the distribution graphs of iVOC and iFF for processed wafers having different texturing recipes and/or various wafer suppliers

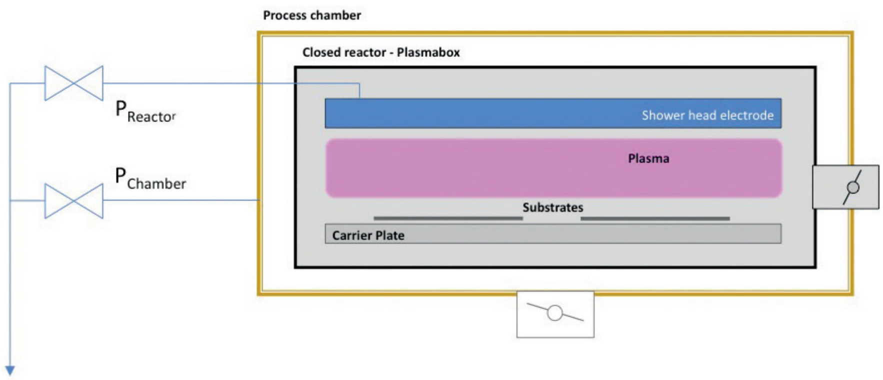

Figure 9: Schematic image of a closed-type RF reactor

Since this treatment has been applied in the standard process routine for HJT cell architectures, several thousand of wafers have been processed, including a variety of different texturing recipes and different wafer suppliers. Figure 8 shows the statistical distribution of the parameters iVOC and iFF. The high mean values demonstrate the robustness of the contamination removal treatment across the board.

Specific OCTOPUS system design features for supporting the suppression of cross contamination

With reference to table 1, item 2, impurities originated by tools, there are some OCTOPUS design features worth highlighting and which definitely support the suppression of potential cross contamination effects.

Adaption of investigated treatment to other PECVD reactor systems:

The treatment method, which was investigated, is applicable to closed reactor designs only. However, since even closed PECVD reactor design concepts are manifold, the specific reactor type should demonstrate its suitability by a test as described above. A principal image of a closed reactor design shows figure 9.

Risk of contamination by internal handling:

Being one of the advantages of the proprietary Mirror Reactor concept, which allows the deposition from the top in one reactor and from the bottom in a second reactor, the OCTOPUS system design does not need any extensive wafer handling or flipping automation, hence any potential contamination risk by wafer touching simply does not exist, see figure 10.

Risk of contamination by tray-carrying-on:

Another advantage of the Mirror Reactor in terms of risk reduction of contamination is related to the exposure of the wafer-carrying tray. Provided that the tray is always fed in to the system with the same side facing up, the tray being coated from previous cycles, will never see the “wrong” plasma deposition side, i.e. the side with potential i-p coatings. Please note that boron will always be removed between cycles, as described above, will never face the plasma side of the i-n coating and vice versa. Any coating mixture of i-p and i-n stacks by several cycles on the carrier is completely avoided with this design.

Impact of OCTOPUS design features and ACCT (Anti Cross Contamination Treatment) on the Cost-of-Ownership bill

System footprint and system utilisation, the specific share of time during which the tool actually adds value to the product, are two of those key tool parameters, which define

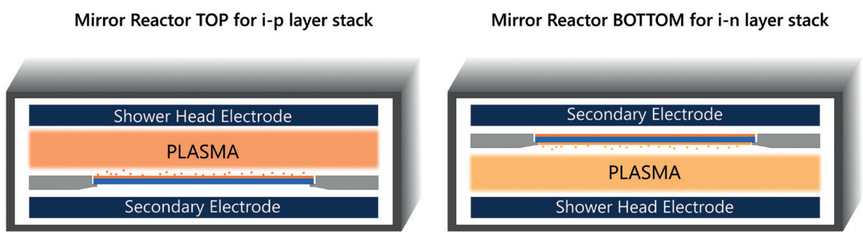

Figure 10: schematic drawing of Mirror Reactor principle incl. carrier loading

the system productivity. Figure 11 illustrates how and to which extent the Mirror Reactor Concept and the ACCT method influence these parameters in a beneficial way.

The OCTOPUS design innovations combined with the Anti Cross Contamination Treatment ACCT result in a superior system utilization rate beyond 75%, a benchmarking value for PECVD systems of this kind, see figure 12.

The conversion cost analysis for the Cost-of-Ownership of a PECVD system of normalized throughput (2400 wafers/hr nominal) provides the following result, figure 13.

Conclusion

The investigation of potential harmful cross contamination by dopants reveals that a highly efficient removal treatment method was found and applied, which successfully suppresses degradation effects due to incorporation dopant impurities into intrinsic layer surfaces. This could be confirmed by a long-term test run showing no sign of any impact even after 100 cycles.

The ACCT treatment method and the OCTOPUS design features, especially of the Mirror Reactor, provide a very reliable PECVD equipment solution to the PV cell market, which successfully demonstrated the suppression of potential cross contamination risks even in a volume production scale.

As a further benefit we could demonstrate to deposit i-p and i-n layer stacks, respectively, in a single reactor, which reduces the number of deposition chambers by half and thus remarkable reduces system footprint and inherited CAPEX.

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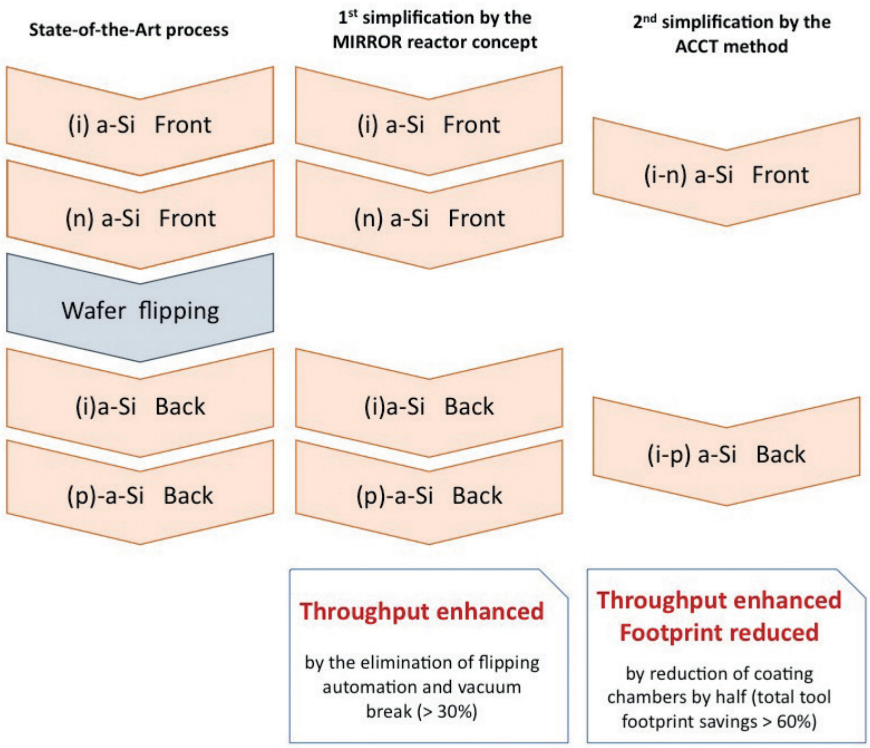

Figure 11: Overview of OCTOPUS cost reduction features

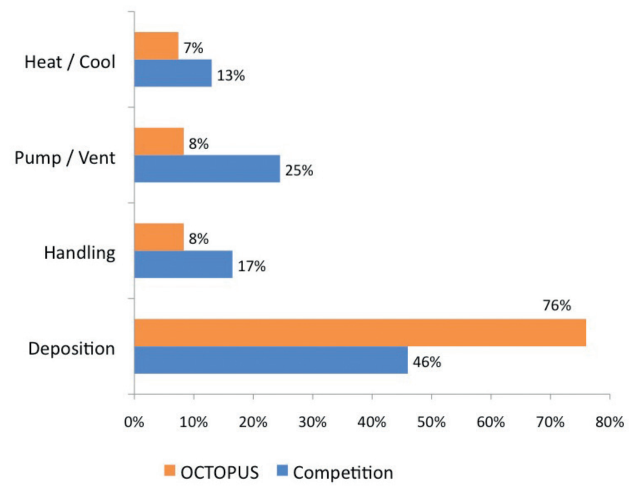

Figure 12: Comparison of the utilization rate between the OCTOPUS and a competitive PECVD system

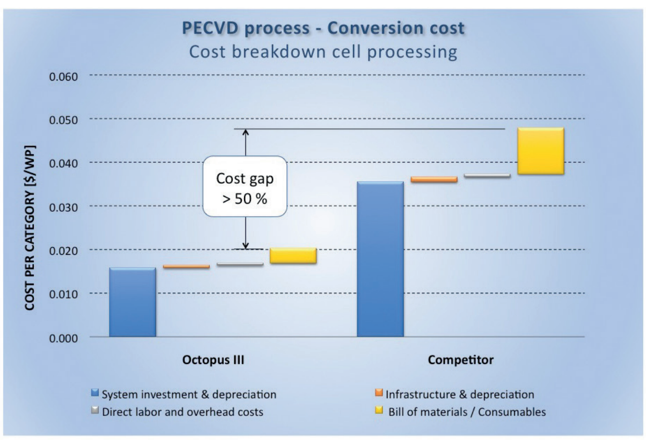

Figure 13: Comparison of the conversion cost-of-ownership for the PECVD process of a HJT cell